USB 3.1 SuperSpeed flash drives for industrial/embedded applications

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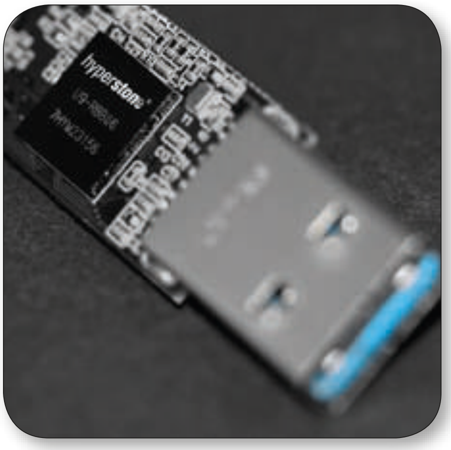
This article introduces the new U9 USB 3.1 NAND Flash Controller combining USB SuperSpeed with power-fail robustness and reliability for industrial applications. It takes full advantage of the increased host interface performance, without any trade-off on the durability and reliability of the solution.



■ In terms of removable flash storage, USB is one of the most popular protocols and USB drives are widely used in consumer markets. Recently, USB is also gaining popularity in industrial applications. Based on a certified interface it shows little field compatibility issues and establishes a fairly robust connection compared to some other interfaces. Where Compact Flash (CF) has been the leading and very reliable interface in the past years, USB is gaining ground, not only as a removable form factor, but especially as embedded USB module or directly soldered on a PCB as disk-on-board solution.

Besides reliability and data retention, read/write speeds are becoming more important. USB 2.0 solutions might not offer sufficient performances. Also notably, access pattern have great impact on flash system lifetime and consumer graded products may fail in the field. In-car infotainment, gaming or network communications, for example, are fields of application, which require fairly high transfer rates and very low read latency.

To address the requirements of these markets, Hyperstone is presenting its updated product line of NAND flash controllers. With USB 2.0, the system bottleneck was the USB interface for a flash system rather than the NAND flash interface. U9 is the latest Hyperstone USB controller adopting USB 3.1 Gen 1 (SuperSpeed 5 Gbps). With 2 NAND flash channels and up to 8 chip enables, it reaches sequential write performance of up to 150 MBps, and sequential read performance of up to 200 MBps. It benefits from the hyReliability flash management features already implemented on previous Hyperstone designs as well as from the latest hyMap technology for higher random write performances and increased endurance. Hyperstone is also in the process of providing an Application Programmers Interface (API) and library enabling its customers to develop their own value-added differentiators and proprietary firmware extensions.

U9 architecture follows a long line of flash memory controller designs developed by Hyperstone targeting industrial and embedded markets. Around an AHB bus and its own 32-bit RISC processor, it includes: USB 2.1 and 3.1 Gen 1 device interface and dedicated PHYs including 2 channels NAND flash interface comprised of: Direct Flash Access (DFA) control co-processor, Flexible Error Correction Coding (ECC up to 96-bits/1KB), AES on-the-fly encryption/decryption engine, and dedicated page buffers for each channels. A number of additional interfaces using a bank of GPIOs (I2C, SPI, GPIO) is also integrated. USB 3.1 Gen1 can be confusing, but this is the official name. However, it was more commonly known as USB 3.0 (5 Gbps interface). Due to various NAND flash technologies (SLC, MLC, TLC, 3D NAND…) different requirements in terms of flash handling are necessary. While process geometries are getting smaller to reduce flash cost, data retention of data stored and endurance in terms of write/erase cycles are getting worse. Over the last years, customers enjoyed continuous cost reductions regarding USD/GByte but as flash memory vendors approach process limitations, reliability is pushed to the limits. In demanding markets, reliability, and power-fail safety are issues to be taken care of since there is a higher cost of non-conformance.

Power fail safety is a key issue for systems requiring reliable data storage but facing unpredictable power downs or being hot-plugged. If the storage media is used to store code, cost of being offline or requiring unscheduled service should be considered. Unlike most SSD controllers, offering comparable performance and endurance, Hyperstone controllers do not require external memory components to store mapping data and FTL metadata. Protecting external DRAM against power-fail requires additional power back-ups such as battery or supercaps in order to save management data when a sudden power-fail occurs. Aside of cost, such components also add to quality, wear-out and endurance weaknesses.

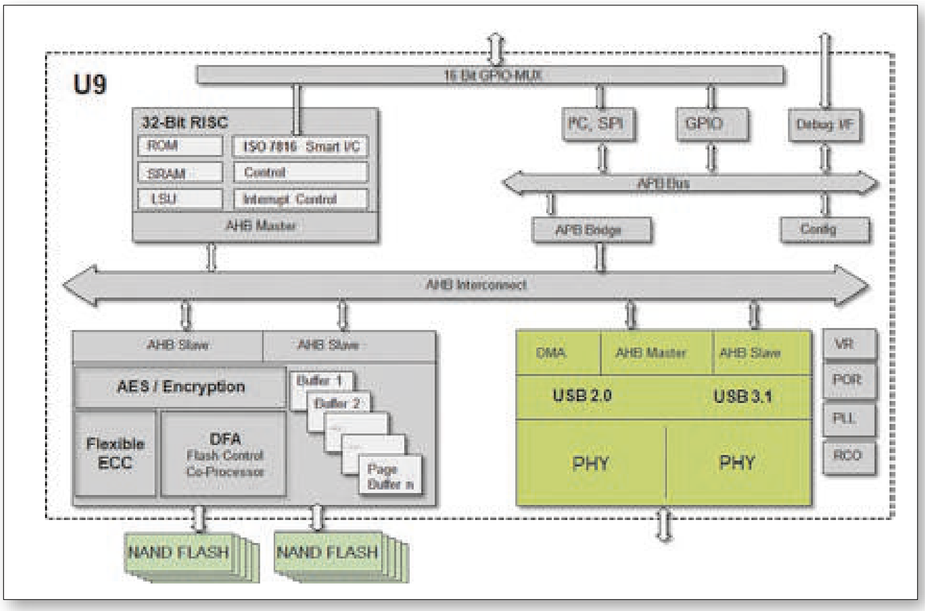
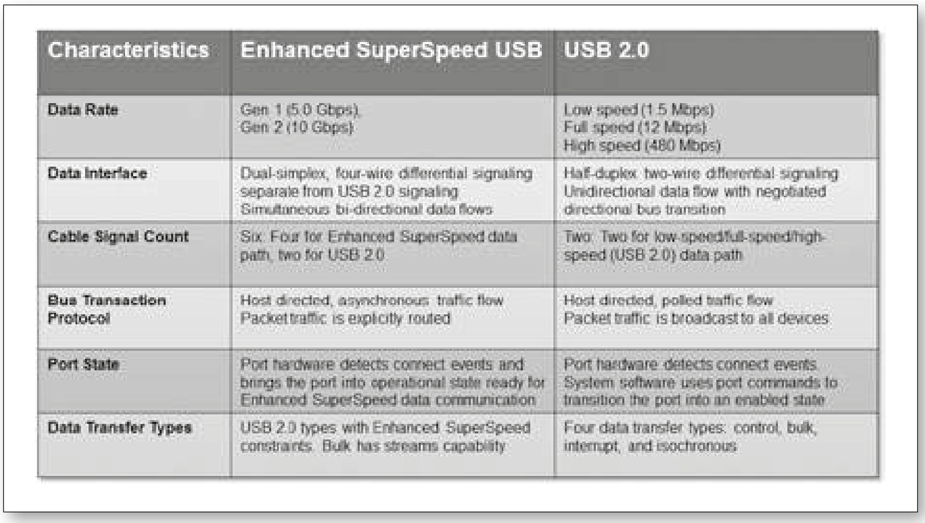


Figure 1. Hyperstone U9 - USB 3.1 Block Diagram



Characteristics	Enhanced SuperSpeed USB	USB 2.0
Data Rate	Gen 1 (5.0 Gbps), Gen 2 (10 Gbps)	Low speed (1.5 Mbps) Full speed (12 Mbps) High speed (480 Mbps)
Data Interface	Dual-simplex, four-wire differential signaling separate from USB 2.0 signaling Simultaneous bi-directional data flows	Half-duplex two-wire differential signaling Unidirectional data flow with negotiated directional bus transition
Cable Signal Count	Six: Four for Enhanced SuperSpeed data path, two for USB 2.0	Two: Two for low-speed/full-speed/high-speed (USB 2.0) data path
Bus Transaction Protocol	Host directed, asynchronous traffic flow Packet traffic is explicitly routed	Host directed, polled traffic flow Packet traffic is broadcast to all devices
Port State	Port hardware detects connect events and brings the port into operational state ready for Enhanced SuperSpeed data communication	Port hardware detects connect events. System software uses port commands to transition the port into an enabled state
Data Transfer Types	USB 2.0 types with Enhanced SuperSpeed constraints. Bulk has streams capability	Four data transfer types: control, bulk, interrupt, and isochronous

Table 1. Comparing USB 3.1 to USB 2.0
(Source: Universal Serial Bus 3.1 Specification, Rev. 1.0, July 26. 2013, chapter 3.1.4)

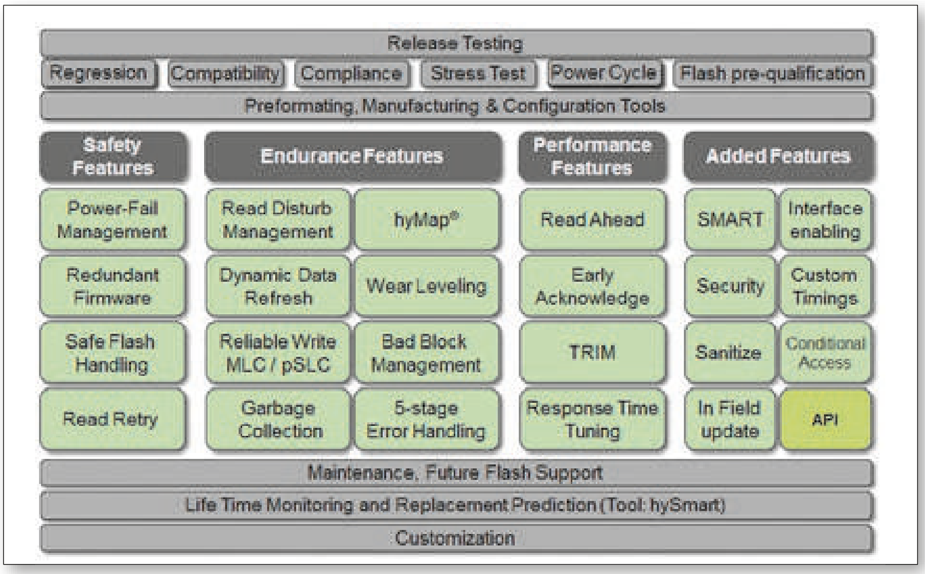


Figure 2. Hyperstone hyReliability firmware features API and Security.

Depending on the flash generation, flashes require a certain number of bits to be correctable by the controller. U9 corrects up to 96 bit errors per 1KB data unit. During Read, the ECC information is used to identify decreasing data quality, wrong bits are corrected and flawless information is send to the host. As soon as a certain threshold of bits that need to be corrected is reached, the entire block is refreshed immediately after error correction and without impacting the overall device performance. This so-called Near-Miss ECC feature is standard in the U9.

Bit errors occur for several different physical reasons: Data retention and program disturb are most common but more recent flashes also need to be protected against read disturbs. Therefore, Hyperstone developed an algorithm (threshold and triggers can be defined by vendors) that frequently checks the data of the entire flash system. Depending on error patterns, individual blocks, areas, or the entire system is refreshed. The U9 firmware analyses the error pattern in order to optimally refresh data without unnecessary performance or wear-out impact. This ensures longest lifetime, data integrity and reliability of the device. For the unusual case that the ECC is not able to correct errors in the data read from a flash, Read Retry is applied. With this function it is possible to recover data by repeating reads on the same cells but with different flash threshold setups. Reading with dynamic read thresholds can dramatically increase flash endurance.

5-stage error handling describes a combination of single features of the U9 to make the flash drive as safe as possible. It therefore combines the basic error correction with additional features like Near-Miss ECC, Dynamic Data Refresh, Read Retry and additional CRC (cyclic redundancy check) protection. The process of the error handling is optimized in a way that: 1) Standard ECC corrects up to 96 bits depending on flash requirements; 2) Near Miss ECC identifies a certain level of errors; 3) Data on the flash is refreshed by the controller and correct data is ensured by double-checking with a CRC check; 4) If the number of errors is greater than the maximum capacity of the ECC, Read Retry is started; 5) To cope with extreme read intensive situations, which may have negative influence on the flash, Dynamic Data Refresh is used to refresh data based on the actual error situation on the whole drive.

The U9 feature Device Health Data - SMART allows users to retrieve data about the health status of the drive. Important parameters related to wear-out or erase cycles, bit error occurrences, read counts etc explain the current health situation on the drive. It gives clear indications whether immediate actions are required or not. This allows the user to run

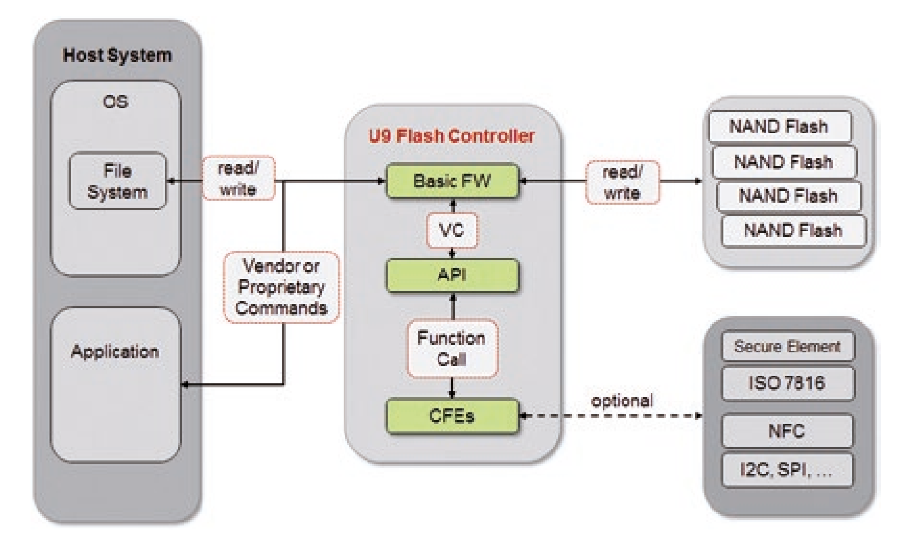
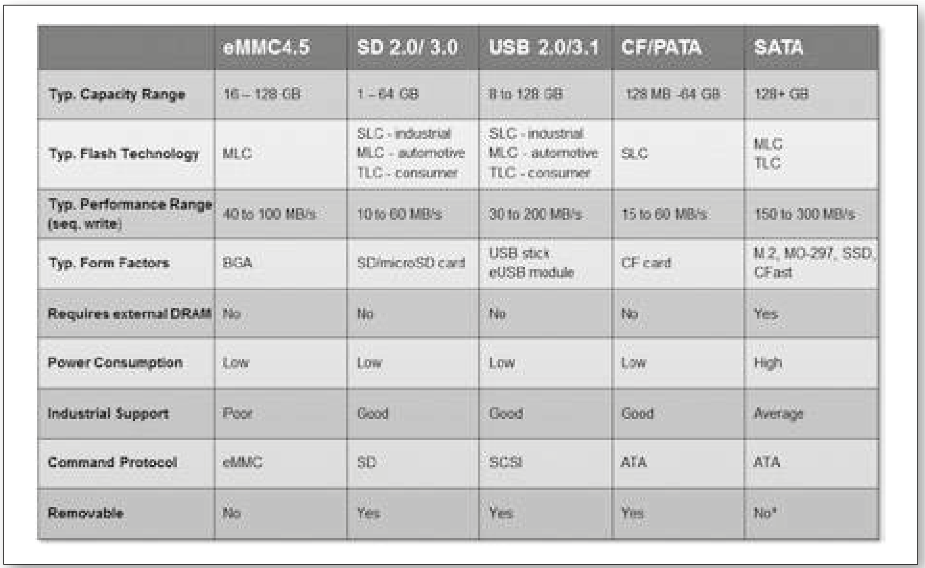


Figure 3. API Block Diagram



	eMMC4.5	SD 2.0/ 3.0	USB 2.0/3.1	CF/PATA	SATA
Typ. Capacity Range	16 – 128 GB	1 – 64 GB	8 to 128 GB	128 MB -64 GB	128+ GB
Typ. Flash Technology	MLC	SLC - industrial MLC - automotive TLC - consumer	SLC - industrial MLC - automotive TLC - consumer	SLC	MLC TLC
Typ. Performance Range (seq. write)	40 to 100 MB/s	10 to 60 MB/s	30 to 200 MB/s	15 to 60 MB/s	150 to 300 MB/s
Typ. Form Factors	BGA	SD/microSD card	USB stick eUSB module	CF card	M.2, MO-297, SSD, CFast
Requires external DRAM	No	No	No	No	Yes
Power Consumption	Low	Low	Low	Low	High
Industrial Support	Poor	Good	Good	Good	Average
Command Protocol	eMMC	SD	SCSI	ATA	ATA
Removable	No	Yes	Yes	Yes	No*

Table 2. Comparison of selected flash storage for removable and embedded flash media

(*) except for CFAST

the flash drive as close as possible or acceptable to the end of the lifetime and to integrate health information into own service plans. Hyperstone flash memory controllers contain dedicated firmware (hyMap) to handle the flash memory. Above and beyond a bridge between a disk interface and a flash memory interface, it is the key element for managing the flash media in order to ensure and maximize its performance, reliability, robustness and endurance. Based on a new development, customers and storage system vendors are enabled to integrate their own proprietary IPs, which may become key product differentiators. The Application Programming Interface (API) provides a possibility to extend the standard firmware and add own additional features to handle other sensitive aspects of the application (for example security features), through a set of routines, protocols and tools. It allows adding customer firmware extensions (CFE) to an existent Hyperstone firmware implementation. This is done by building (compiling and linking) an independent binary file, which is able to communicate with a host software and with the basic flash firmware.

Custom applications can be developed independently of the Flash Memory controller firmware. As a result, the CFE will be part of the firmware code and will be integrated alongside the other firmware features. The API can be used to provide access to additional hardware interfaces through the host interface in order to implement customized application features. The source code can be changed individually, always belongs to the user and does not need to be transferred to Hyperstone for compilation. The key advantages for the customer can be summarized in the following set of added values: full control of application IPs, full control of releases, no source code transfer to third party houses, unique differentiator through application IPs, fast software development, API function support from Hyperstone, and Firmware Field Update (FFU).

The U9 USB 3.1 controller complements the Hyperstone product portfolio of Flash storage controllers as USB 3.1 is a suitably alternative to CF, SD, eMMC or SATA systems. Together with hyMap® - Hyperstone's Flash-Translation layer (FTL), and the hyReliability feature set, U9 optimally ensures and balances reliability, endurance and performances. Based on several configuration options, storage system integrators can decide about most suitable and most cost efficient Flash technologies and tune storage system behavior to application requirements. Finally, by offering an API, Hyperstone promotes a new feature and value added application development based on the existing flash support infrastructure and ecosystem.■