Choosing the right embedded flash disk for various applications

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This article describes how flash controllers can be used to directly embed flash drives onto PCBs and into systems. Hidden bill-of-material (BOM) costs can be avoided and control over component lifetimes maximized. Drives can be configured according to the application-specific requirements.

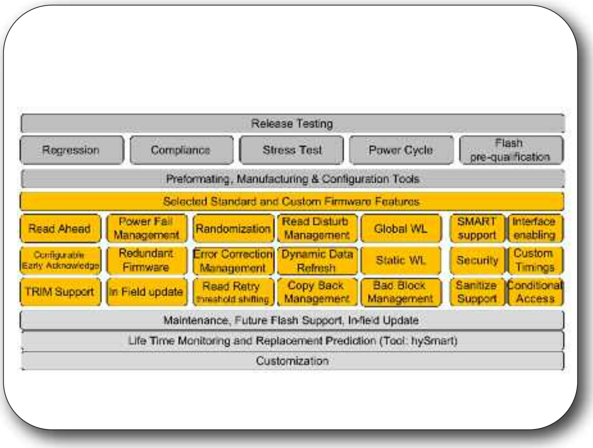
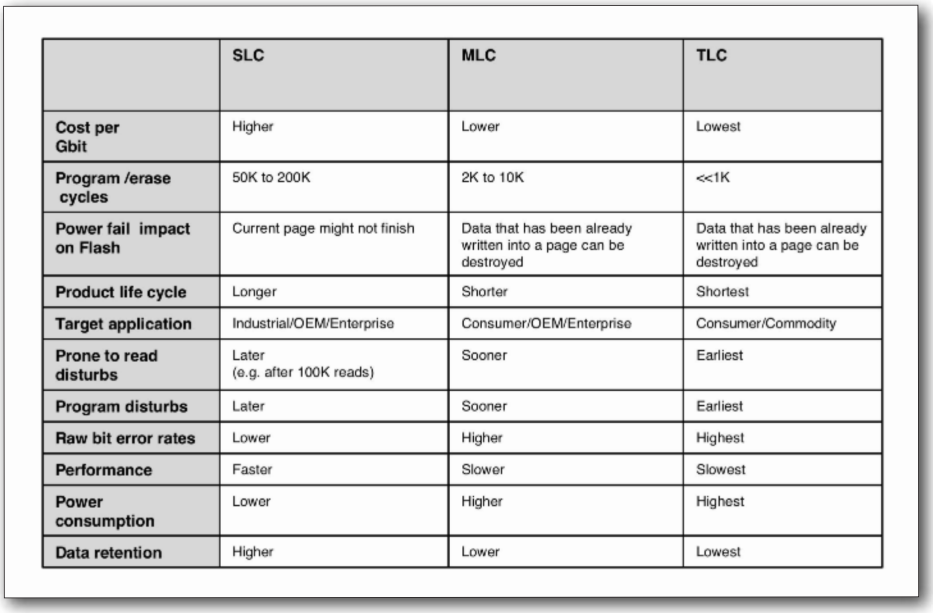


Figure 1. Hyperstone hyReliability Firmware architecture - selected modules

■ At the Embedded World 2013, Hyperstone is presenting their updated product line-up of NAND flash controllers including SATA and SD 3.0 controllers. Together with hyReliability firmware, embedded designers can easily realize embedded flash directly on-board. Designers are facing an increasing number of options when designing an application that requires mass storage. Depending on requirements, the trade-offs in terms of cost per bit, quality, life cycle cost, and maintenance are significant. HDDs still offer the best cost per bit. However, for an increasing number of applications, local storage is flash-based since NAND flash offers several advantages. Many different NAND-based standard products are available from solid state disks (SSD) to flash memory cards (e.g. SD cards, CompactFlash cards and USB flash disks) to embedded flash multichip packages (MCP) such as eMMC. Significant differences in terms of cost, capacity, performance, quality, reliability, and power consumption relate to flash process, controller, and firmware technology.

NAND memory technologies today include single level cells (SLC), multi-level cells (MLC) and three level cells (TLC). These technologies differ in how many bits of information (levels) are attributed to different numbers of electrons pushed into a floating gate. More levels mean fewer electrons associated to a bit of information. Fewer electrons mean more errors and less data retention. Also, physical stress to each memory cell is increased the more electrons need to be pushed in and out of the floating gate as it is being programmed or erased. Hence, the specified lifetime in program-erase cycles (PE cycles) is much smaller for TLC than for SLC, for example. Finally, the likelihood of disturbances resulting from operations to neighbouring cells or as an exposure to heat increases. All those effects get worse and more significant as manufacturing process technology shrinks. All these effects result in faster cell wear-out, less data retention, longer program times, and higher power consumption.

Of course, higher information density per chip area is cheaper. Since most NAND flash providers have to fight for cost leadership per mm2 chip area and the main volume is in consumer markets, cost optimization is focusing on MLC and TLC. Hence MLC product life cycles are shorter and usually MLCs available are already in smaller geometries compared to the comparable SLC available at the same time. For instance, today you might consider 1x MLC or 2x SLC. At the same time, today you can still buy 4x and 3x SLC, but 2x MLCs are already difficult to procure. TLC reliability parameters are not suited for embedded designs, which can be derived from table 1. Consumer products have been offering sufficient quality and endurance for many applications with increased reliability requirements in the past. In the future, they are likely to fail since they have been designed to satisfy other requirements. Beyond being a bridge between two interface protocols, the firmware is responsible for managing the flash media including error handling, power fail recovery, countermeasures against wear-out, and optimal usage of all flash cells, to name a few examples. The firmware has to continuously make arbitrary decisions regarding performance, wear-out, robustness and data retention. As an example, one physical effect that has become more significant recently is the so-called read disturb. This refers to the phenomenon of when a specific sector of one page is read and another sector of another page that is neighbouring on the flash physical topology is impacted. After a certain number of reads, this other sector might deliver significant bit errors, eventually exceeding the controller ECC strength. This has an impact on the stored firmware itself, parts of the OS or files system, or possibly application data that is read repeatedly. The firmware can address this phenomenon by refreshing certain areas based on read counts of other areas. To do so, the phenomenon has to be assessed for each flash. Afterwards, a refresh procedure has to be implemented trying to minimize performance penalty or additional programming overhead which

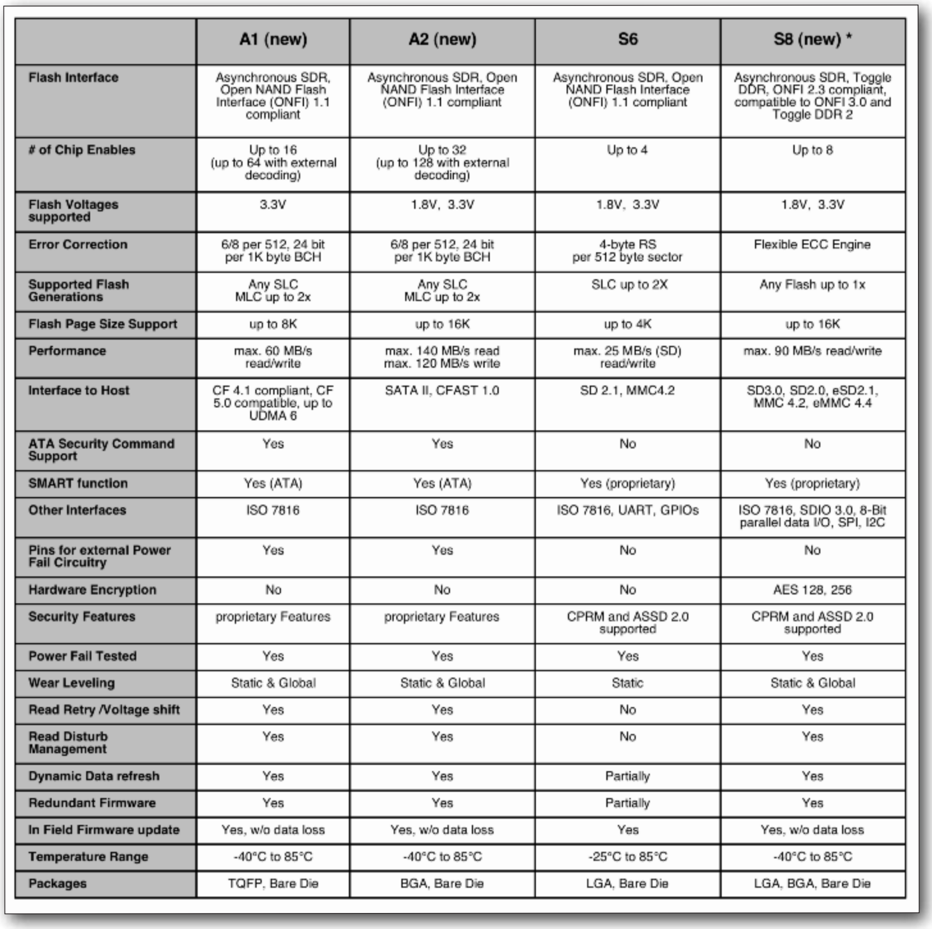


	SLC	MLC	TLC
Cost per Gbit	Higher	Lower	Lowest
Program /erase cycles	50K to 200K	2K to 10K	<<1K
Power fail impact on Flash	Current page might not finish	Data that has been already written into a page can be destroyed	Data that has been already written into a page can be destroyed
Product life cycle	Longer	Shorter	Shortest
Target application	Industrial/OEM/Enterprise	Consumer/OEM/Enterprise	Consumer/Commodity
Prone to read disturbs	Later (e.g. after 100K reads)	Sooner	Earliest
Program disturbs	Later	Sooner	Earliest
Raw bit error rates	Lower	Higher	Highest
Performance	Faster	Slower	Slowest
Power consumption	Lower	Higher	Highest
Data retention	Higher	Lower	Lowest

Table 1. High-level comparison of SLC, MLC and TLC NAND memory technologies

again would add to wear-out. Also, this might lead to busy times not expected by the hosts.

Another significant and often discussed feature is wear levelling. The principle is to use all pages/blocks of a flash evenly. A so-called logical to physical mapping is required and managed by the firmware. This mapping, if you look at it in detail, is quite complex. Depending on the administrative architecture being based on blocks or pages, the mapping tables differ in size to an extent that either requires hundreds of MB external DRAM (page-based) or sufficient to be using internal SRAM (block-based). Each approach has certain trade-offs in terms of power-fail robustness or performance. It might be beneficial to use a "local" wear levelling approach that manages only a single flash in order to make use of certain performance features of the flash such as copy back. While this increases system performance, it results in one flash chip deteriorating faster than others within the system. The global wear levelling approach uses all chips but cannot utilize the copy back feature.



	A1 (new)	A2 (new)	S6	S8 (new) *
Flash Interface	Asynchronous SDR, Open NAND Flash Interface (ONFI) 1.1 compliant	Asynchronous SDR, Open NAND Flash Interface (ONFI) 1.1 compliant	Asynchronous SDR, Open NAND Flash Interface (ONFI) 1.1 compliant	Asynchronous SDR, Toggle DDR, ONFI 2.3 compliant, compatible to ONFI 3.0 and Toggle DDR 2
# of Chip Enables	Up to 16 (up to 64 with external decoding)	Up to 32 (up to 128 with external decoding)	Up to 4	Up to 8
Flash Voltages supported	3.3V	1.8V, 3.3V	1.8V, 3.3V	1.8V, 3.3V
Error Correction	6/8 per 512, 24 bit per 1K byte BCH	6/8 per 512, 24 bit per 1K byte BCH	4-byte RS per 512 byte sector	Flexible ECC Engine
Supported Flash Generations	Any SLC MLC up to 2x	Any SLC MLC up to 2x	SLC up to 2X	Any Flash up to 1x
Flash Page Size Support	up to 8K	up to 16K	up to 4K	up to 16K
Performance	max. 60 MB/s read/write	max. 140 MB/s read max. 120 MB/s write	max. 25 MB/s (SD) read/write	max. 90 MB/s read/write
Interface to Host	CF 4.1 compliant, CF 5.0 compatible, up to UDMA 6	SATA II, CFAST 1.0	SD 2.1, MMC4.2	SD3.0, SD2.0, eSD2.1, MMC 4.2, eMMC 4.4
ATA Security Command Support	Yes	Yes	No	No
SMART function	Yes (ATA)	Yes (ATA)	Yes (proprietary)	Yes (proprietary)
Other Interfaces	ISO 7816	ISO 7816	ISO 7816, UART, GPIOs	ISO 7816, SDIO 3.0, 8-Bit parallel data I/O, SPI, I2C
Pins for external Power Fail Circuitry	Yes	Yes	No	No
Hardware Encryption	No	No	No	AES 128, 256
Security Features	proprietary Features	proprietary Features	CPRM and ASSD 2.0 supported	CPRM and ASSD 2.0 supported
Power Fail Tested	Yes	Yes	Yes	Yes
Wear Leveling	Static & Global	Static & Global	Static	Static & Global
Read Retry /Voltage shift	Yes	Yes	No	Yes
Read Disturb Management	Yes	Yes	No	Yes
Dynamic Data refresh	Yes	Yes	Partially	Yes
Redundant Firmware	Yes	Yes	Partially	Yes
In Field Firmware update	Yes, w/o data loss	Yes, w/o data loss	Yes	Yes, w/o data loss
Temperature Range	-40°C to 85°C	-40°C to 85°C	-25°C to 85°C	-40°C to 85°C
Packages	TQFP, Bare Die	BGA, Bare Die	LGA, Bare Die	LGA, BGA, Bare Die

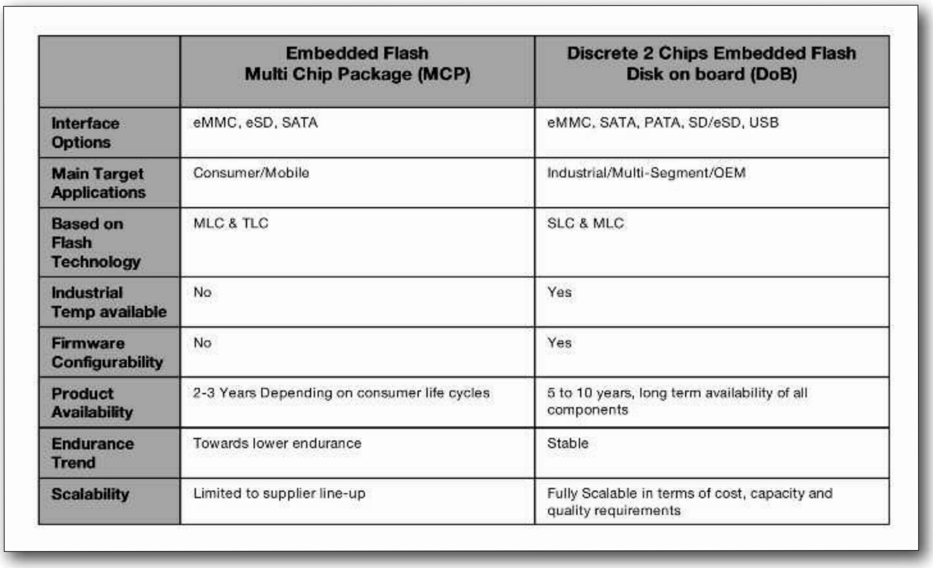
Table 2. Hyperstone product overview (SD, eMMC, PATA and SATA) suited for embedded flash disk on board

Another example of a non-trivial decision is the consideration and interpretation of bit errors. The firmware can define several bit error thresholds after how many bit errors a page or block could be refreshed, copied, retired and mapped out assuming it has reached the end of its useful life. Many flash systems show performance degradation over their lifetime. The reason is not only the increased ECC activity due to deteriorated flashes but also the fact that an increased amount of housekeeping and maintenance operations are being executed in the background.

These are just a few examples of many features that are not transparent in their implementation but can have a significant impact for an application over their operating life time. The impact of flash generation changes or any firmware change can be significant, making it challenging to qualify a flash system for an application. This tremendous firmware effort is one reason why connecting raw NAND or even NAND with added ECC hardware is not efficient for many applications. When qualifying and managing product changes of a managed NAND option such as an eMMC, you might want to monitor flash, controller and firmware versions as part of a bill of materials that might be partially hidden and not easily transparent.

Integrating modules or cards such as CompactFlash cards, SD cards, USB flash disks, or solid state disks, is certainly the most flexible option. Most standard interfaces are available in some standard form factor. The module or card manufacturer is part of the value chain and takes care of flash and controller procurement, system and PCB design, manufacturing including firmware preformatting as well as life cycle management and warranty. With respect to flash systems, these are very valuable services. Independent of the mainboard life cycle, modules or cards are removable. Updates can be quite easily accommodated. With one qualification cycle you can roll out new revisions over several applications or platforms.

However, for cost optimization of a stable application with certain volumes or for space considerations, it might make sense to integrate



	Embedded Flash Multi Chip Package (MCP)	Discrete 2 Chips Embedded Flash Disk on board (DoB)
Interface Options	eMMC, eSD, SATA	eMMC, SATA, PATA, SD/eSD, USB
Main Target Applications	Consumer/Mobile	Industrial/Multi-Segment/OEM
Based on Flash Technology	MLC & TLC	SLC & MLC
Industrial Temp available	No	Yes
Firmware Configurability	No	Yes
Product Availability	2-3 Years Depending on consumer life cycles	5 to 10 years, long term availability of all components
Endurance Trend	Towards lower endurance	Stable
Scalability	Limited to supplier line-up	Fully Scalable in terms of cost, capacity and quality requirements

Table 3. Comparison of embedded flash as MCP or discrete disk on board (DoB)

and embed a flash-based mass storage sub-system directly as an MCP on board. Such modules are available mostly in BGA packages and are more or less standardized, e.g. with eMMC or SATA interfaces. However, since most are developed for consumer markets, cost might be attractive but suitability for other applications and extended requirements might be questionable. Another alternative is integrating flash controller and flash as two discrete components. This has certain benefits especially for industrial embedded applications.

Based on Hyperstone products, it is easy to implement an embedded flash disk onto a PCB and into systems. Chip hardware, fully qualified to industrial requirements, is available together with the most reliable firmware. Reference design schematics, configuration tools as well as local support will help you to optimize firmware for your specific requirements. Controlled or even fixed BOM is fully under control. Once a setup has been qualified, the requalification effort can be minimal. The impact of reacting to any flash EOL is smaller since controller and firmware might not need to be changed. Hyperstone currently offers flash controllers supporting any type of flash technology and interfacing to SATA, PATA and SD or MMC hosts. Another advantage is long term availability. Certain Hyperstone controllers have been available for more than 10 years, and support for new flash memories continues to be added today.

When qualifying a storage system that includes NAND flash, controller, and firmware, the firmware version is also an important factor for qualification. Hyperstone can support designing an application with an embedded flash storage sub-system integrating controller and NAND flash in parallel. Customization and application specific tuning is possible. In any case, SLC is the flash of choice for reliability and endurance. eMMCs are currently designed and optimized for consumer mobile phones. Since eMMC or embedded flash MCPs are often exposed to cost pressure from consumer markets, changes to flash, controller, and firmware are much faster and usually not announced via product change notes. Long-term availability of qualified industrial products is questionable. Given these constraints, predominantly MLC-based MCPs require a great level of attention to whether the controller, firmware and choice of flash are optimally suited for your application over the whole life cycle. Using a separate controller, NAND flash, and an optimally configured firmware will help applications to be more rugged and the storage sub-system to be better tuned for the target application. Also, life-cycle cost is minimized due to long-term availability of Hyperstone products. The need for frequent changes to products is reduced thus resulting in lower cost for requalification. ■