A2 Flash Memory Controller


hyperstone®


MO-297
CFast™
SSD
embedded Flash
MO-300

# A2

## Flash Memory Controller

The Hyperstone A2 family of Flash Memory Controllers together with provided application and flash specific firmware offers an easy-to-use turnkey platform for high endurance robust flash disks of various form factors and interface standards.

- Smallest and most power efficient SSD controller
- Patented superior read and write wear leveling together with up to 24-Bit ECC ensuring highest reliability and endurance
- Exceptional power fail robustness
- Optimized 32-Bit RISC core, instruction set and firmware for flash handling
- 4 channel controller provides optimal performance for target applications
- Most power efficient design together with power saving features
- S.M.A.R.T. features supported
- Custom features can be implemented with simple firmware upgrades
- ASSP with minimal external active components
- Turnkey solution including firmware, manufacturing kit, test and development hardware, and reference schematics for applications such as 2.5" SATA solid state disk (SSD), MO-297, MO-300, and CFast.

### Targeted Applications

- High reliability & industrial Solid State Disks (SSD) including 2.5" and 1.8" SSD, MO-297, MO-300
- SATA Disk-on-Modules (DoM)
- Embedded Flash
- Multi-Chip-Modules (MCM)
- Multi-Chip-Package (MCP)
- Disk-on-Board

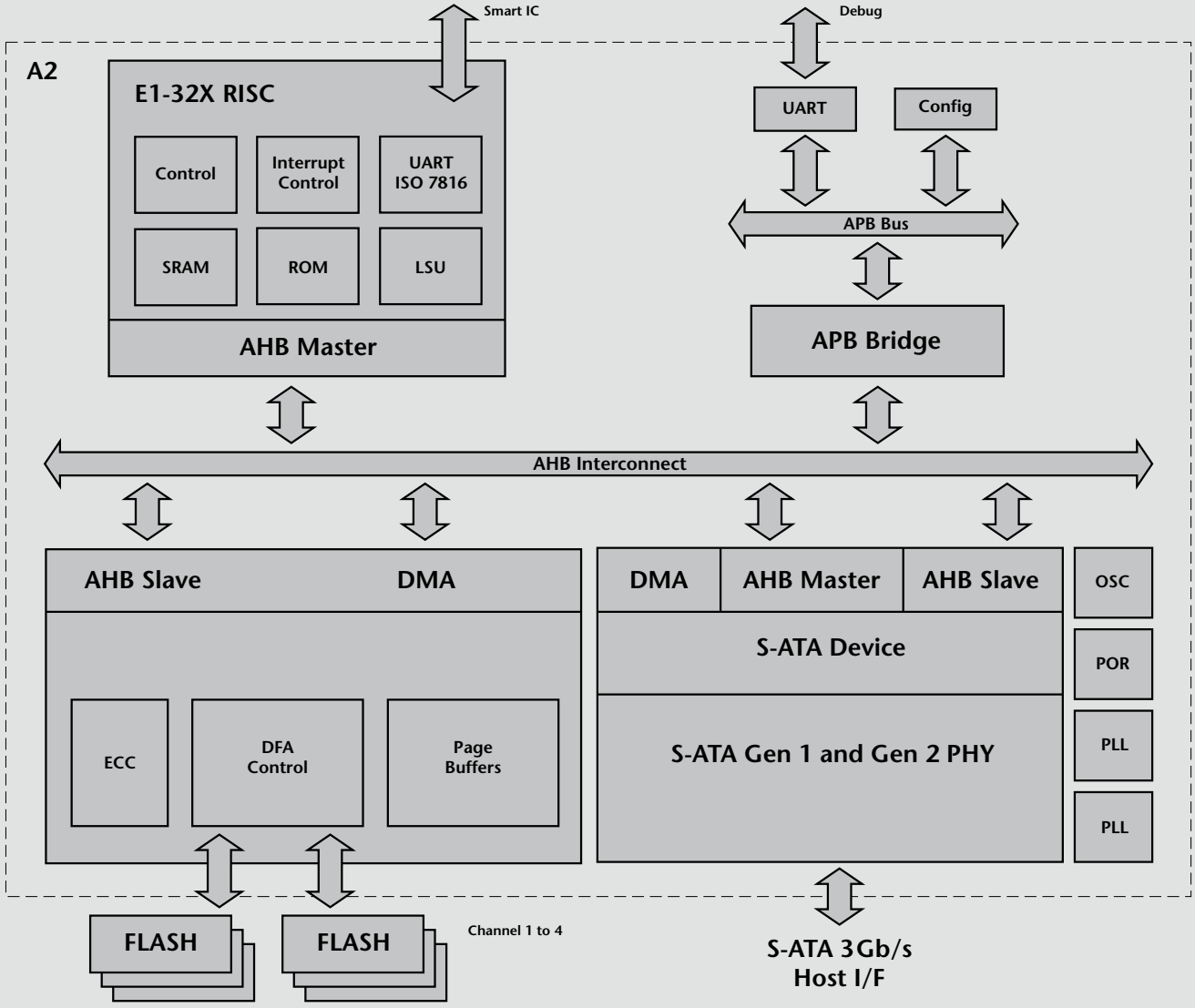
### Order Information

- A2-RAP08 --- TFBGA 201, 9×9×1.2 mm, 0.5 mm pitch, 32 CEs, RoHS, -40 to +85 °C
- A2-RAP09 --- TFBGA 201, 13×13×1.2 mm, 0.8 mm pitch, 32 CEs, RoHS, -40 to +85 °C
- A2-0ABD0 --- Tested Die / Wafer

### Compliance & Performance

- Fully compliant to Serial ATA 2.6 and CFast 1.1 specification
- Fully compliant to ATA-7 and compatible to ATA-8
- SATA partial and slumber power modes and CFast PHYSLP power modes supported
- Native Command Queuing (NCQ)
- Support for SMART Commands
- Up to 300 MB/sec burst transfer speed
- Sustained read up to 150 MB/s
- Sustained write up to 130 MB/s
- 4K random write IOPS: up to 600
- SATA Gen 1 (1.5 Gb/sec) and SATA Gen 2 (3.0 Gb/sec) transfer speeds supported
- Typical active current consumption of about 250mA
- SATA partial/slumber (~150mA) and CFast PHYSLP (~5mA) power modes supported

## A2 Block Diagram



## Controller & CPU

- High performance 32-Bit Hyperstone RISC microprocessor
- Large internal RAM provides firmware flexibility
- Eight GPIO pins for customer specific applications and ISO7816 interface for SmartCard applications
- Unique ID for security applications
- Typical active current consumption (@25°C and 100% utilization during stress test with 4x 3.3V Flashes) of about 250mA
- SATA partial/slumber (~150mA) and CFast PHYSLP (~5mA) power modes supported
- Supply voltage power-down detection for full power-down robustness
- Capacitor buffered power down and write recovery possible
- Supply voltage 1.2V and for Flash I/O: 1.8V or 3.3V
- Flash memory interface supply voltage 3.3V or 1.8V

## Host Interface & Compliance

- Fully compliant with Serial ATA 2.6
- Fully compliant with ATA-7, compatible to ATA-8
- Fully compliant with CFast-1.1
- SATA Gen 1 (1.5 Gb/sec) and SATA Gen 2 (3.0 Gb/sec) transfer speeds supported
- Up to 300 MB/sec burst transfer speed
- SATA partial and slumber power modes and CFast PHYSLP power mode supported
- Native Command Queuing (NCQ) support
- TRIM support
- LBA 48 support to design drives larger than 128GB

## Flash Memory Interface & Handling

- 4 channel with four direct flash memory access (DFA) units including sector buffers and interleaving capability
- Supporting all control signals for NAND type flash memory connection
- Asynchronous SDR interface, ONFI 1.0 compliant and compatible with ONFI 2.x.
- Supporting direct connection of up to 32 flash memory chip enables (CE) - eight per channel
- Flash memory power down logic and flash memory write protect control
- BCH Error Correcting Code (ECC) capable of correcting 6 or 8 Bit in a 512 bytes sector and 24 Bit in a 1024 bytes double-sector with additional CRC
- Supporting all flash technologies MLC and SLC and all page sizes up to 16KB
- Flash management including mapping of logical block addresses (LBA) to corresponding physical block addresses (PBA)
- Bad Block Management
- Minimal Write Amplification
- Static and Global Wear leveling to maximize write endurance
- Inherent on-the-fly garbage collection
- Read Wear leveling to maximize data retention and refresh data subject to read disturbance
- Management of sudden power-fails
- Interleaving, cache, and multi-plane programming
- Firmware is stored in NAND Flash and loaded into internal memory by the boot ROM
- Firmware can be stored redundantly for recovery and for periodic refresh
- Future Flashes can be supported by simple firmware upgrades
- Customized firmware, optimizations and feature implementations possible upon request

**Hyperstone GmbH**
Line-Eid-Strasse 3
78467 Konstanz
Germany
Phone: +49 7531 98030
Email: eu.sales@hyperstone.com

**Hyperstone Inc. - USA**
486 N Patterson Drive Suite 301
Winston-Salem, NC 27101
USA
Phone: +1 336 744 0724
Email: us.sales@hyperstone.com

**Hyperstone Asia Pacific - Taiwan**
3F., No. 501, Sec.2, Tiding Blvd.
Neihu District, Taipei City 114
Taiwan, R.O.C.
Phone: +886 2 8751 0203
Email: ap.sales@hyperstone.com

www.hyperstone.com



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