

S8 Flash Memory Controller

S8

hyperston[®]

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The Hyperstone S8 family of Flash Memory Controllers together with provided application and Flash specific firmware offers an easy-to-use turnkey platform for industrial, high endurance robust Flash Memory cards or modules compatible to host systems with (e)SD or (e)MMC interfaces.

- Designed to satisfy industrial requirements
- **hyReliability™** Flash Management including superior wear leveling, read disturb management, and power fail management ensuring highest reliability and endurance
- **hyMap®** Flash Translation Layer and mapping offering second to none random write performance, minimal write amplification, and consequently highest endurance for random access heavy usage profiles (e.g. JEDEC Enterprise)
- Continuously updated Flash Memory chip support and long term availability
- Flexible ECC engine supporting all Flash Memory requirements
- Optimized 32-Bit RISC core, instruction set for Flash Memory handling
- High performance on-the-fly AES encryption engine
- Custom features can be implemented with simple firmware upgrades
- 16 GPIO for customer specific applications supporting SDIO 3.0, SPI, I²C, and ISO7816
- ASSP with minimal external active components
- Turnkey solution including firmware, manufacturing kit, test and development hardware, as well as reference schematics

Targeted Applications

- SecureDigital (SD) card
- microSD and Smart microSD
- e•MMC
- Legacy MMC and SD cards
- Embedded Flash modules
- Multi-Chip-Package (MCP)
- Disk-on-Board

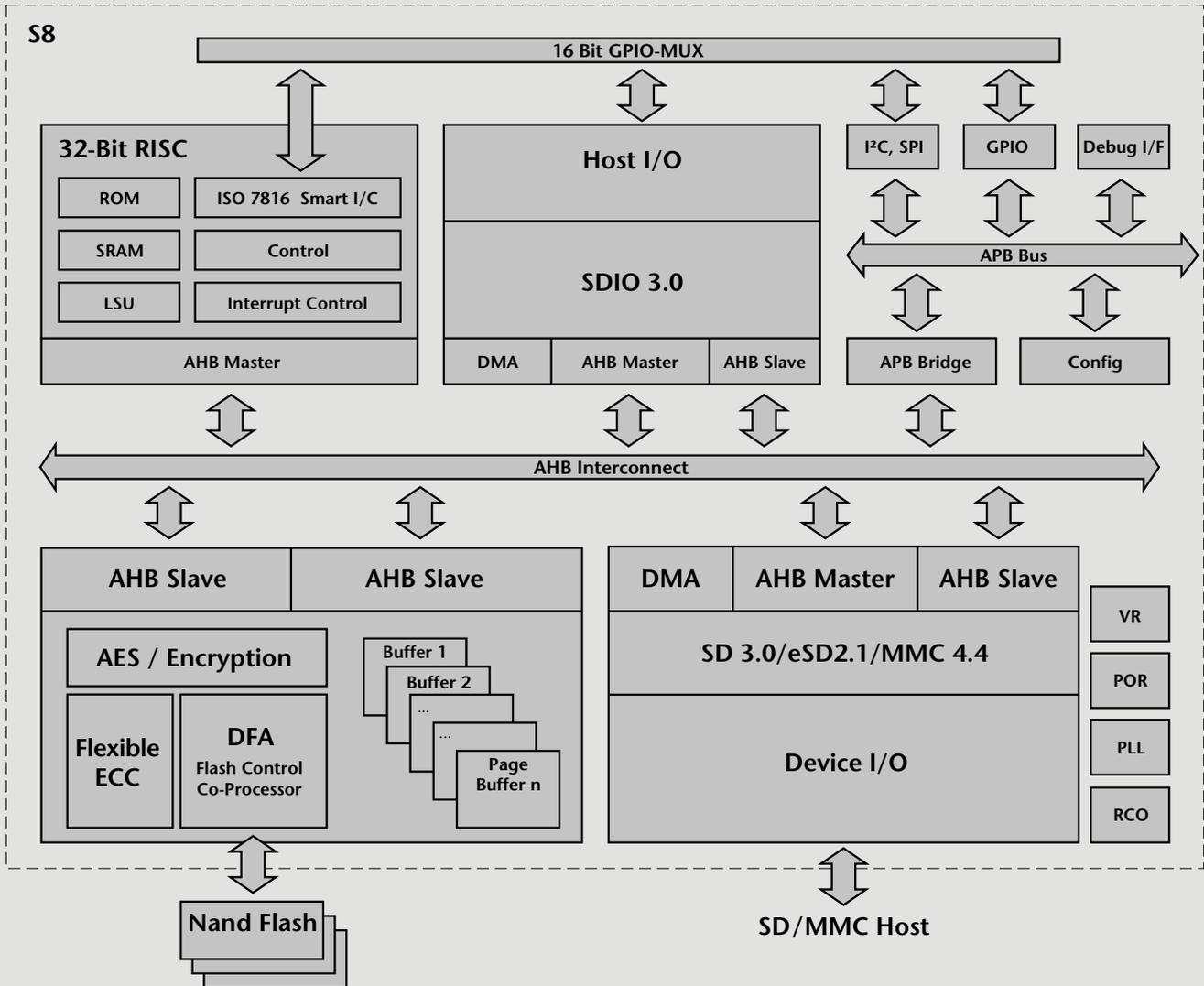
Order Information

- S8-LAK07 --- LGA 52, 7.5 x 4.0 x 0.7 mm, 4 CEs, RoHS, -40 to +85 °C
- S8-0ABD0 --- Tested Die/Wafer

Compliance & Performance

- Fully compliant with SD3.0 (UHS-I), SD2.0, and eSD2.1 specifications
- CPRM and ASSD 2.0 or Mc-EX can be supported
- Fully compliant with e•MMC 4.41, and MMC 4.2 specifications
- Host transfer rate of up to 104 MB/s in SD 3.0 SDR104 and e•MMC 4.4 DDR modes
- Sequential read and write up to 90 MB/s using toggle mode or ONFI 2 SLC Flash
- Sequential read and write up to 60 and 25 MB/s respectively using toggle mode or ONFI 2 MLC Flash
- All SD Speed Classes possible

S8 Block Diagram



Controller & CPU

- High performance 32-Bit Hyperstone RISC microprocessor
- Large internal RAM provides firmware flexibility
- 16 GPIO pins for customer specific applications, multiplexed interface options include: 16 GPIO, SDIO 3.0, SPI, I²C, 4x CE and ISO7816
- Unique ID for security applications
- AES encryption engine 128 and 256-Bit, ECB, CBC, and XTS modes supported, high performance on-the-fly encryption/decryption
- Flexible clock frequency generation through internal oscillator and PLL
- Automatic power-down mode during wait periods for host data or Flash Memory operation completion, automatic sleep mode during host inactivity periods
- On-chip voltage regulator for 1.2V controller core power

Host Interface & Compliance

- Fully compliant with SD3.0 (UHS-I), SD2.0, and eSD2.1
- CPRM and ASSD 2.0 or Mc-EX can be supported
- Fully compliant with eMMC 4.4, and MMC 4.2 specifications
- Supports backward compatible, high speed and DDR modes in eMMC 4.4
- Optional support for eMMC 4.5 features Power-Off Notification, Discard, and Sanitize
- Supports DS, HS, SDR12, SDR25, SDR50, SDR104 and DDR50 modes of SD 3.0
- Host transfer rate of up to 104 MB/s in SD 3.0 SDR104 and eMMC 4.4 DDR modes
- Hardware support for the C2 encryption and decryption functions (CPRM)
- On-chip voltage regulator for 1.8V signalling voltage in SD 3.0 transfer modes

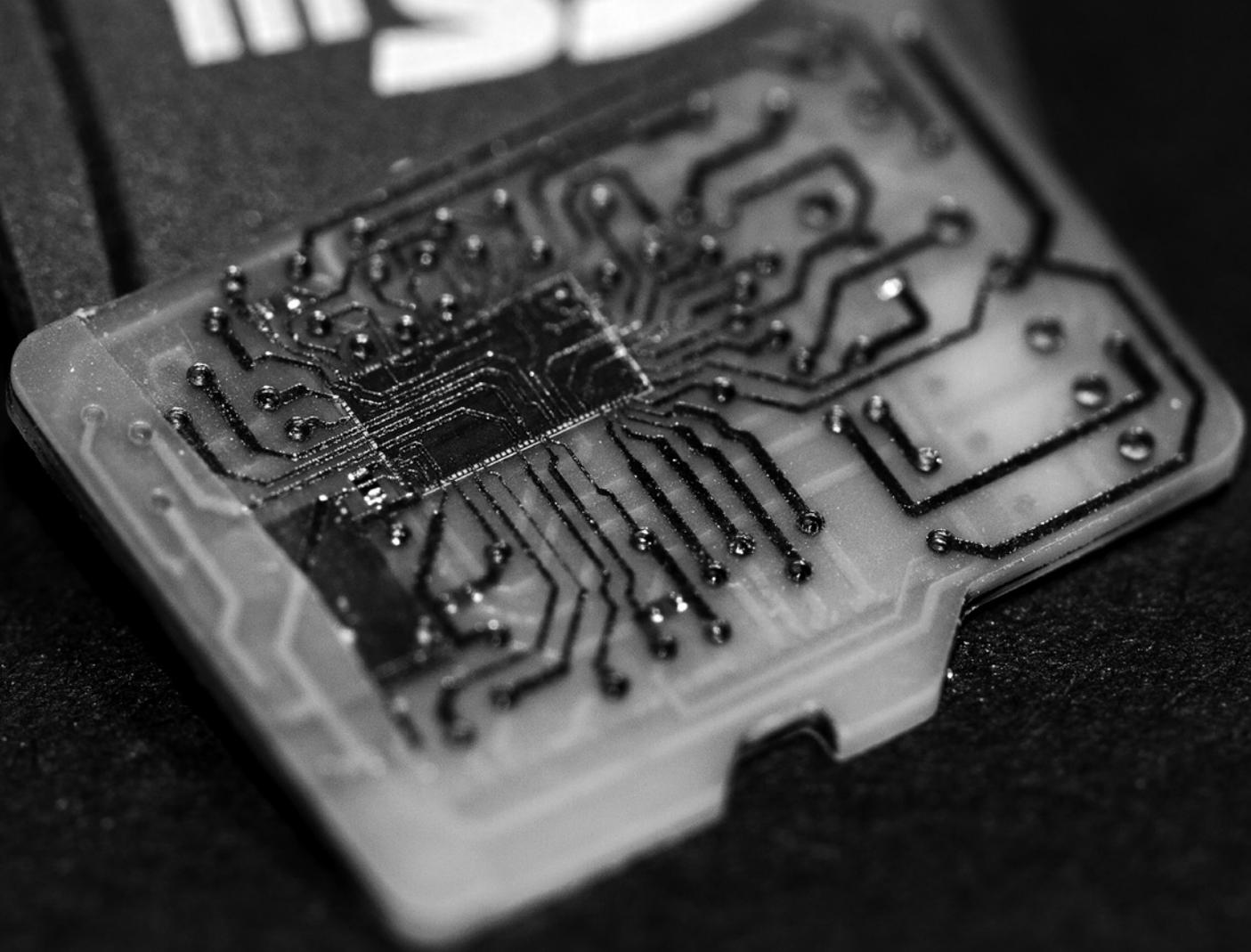
Flash Memory Interface

- Direct Flash Memory Access (DFA) co-processor including page buffers and interleaving capability
- Synchronous DDR interface compliant with Toggle DDR and ONFI 2.1, compatible with all DDR Flash Memory devices
- Asynchronous SDR interface, ONFI 1.0 compliant compatible with all legacy interface Flashes
- Data transfer rate to Flash up to 200 MB/s
- Flexible ECC engine supporting all Flashes
- CRC for additional reliability
- Direct connection of up to 8 Flash Memory chip enables (CE)
- Flash Memory power down logic and Flash Memory write protect control
- Supporting all Flash technologies and all page sizes up to 16KB
- On-chip voltage regulator for 1.8V Flash Memory I/O power

Flash Memory Management

- hyReliability™ Flash Memory Management optimizing reliability, power fail safety, endurance, data retention, and performance
- hyMap® Flash Translation Layer and mapping offering second to none random write performance, minimal write amplification, and consequently highest endurance for random access heavy usage profiles (e.g. JEDEC Enterprise)
- Optimized for fast boot-up times
- Bad Block Management
- Static and Global Wear leveling to maximize write endurance
- Inherent on-the-fly garbage collection
- Read Disturb Management, Dynamic Data Refresh to maximize data retention and refresh data subject to read disturbance
- Management of sudden power-fails
- Interleaving, cache, and multi-plane programming
- Firmware is stored redundantly for recovery and periodic refresh
- In-Field Firmware update without user data loss
- Customized firmware, optimizations and feature implementations possible upon request.

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Hyperstone GmbH

Line-Eid-Strasse 3

78467 Konstanz

Germany

Phone: +49 7531 980 30

Email: eu.sales@hyperstone.com

Hyperstone Inc. - USA

486 N Patterson Ave Suite 301

Winston-Salem, NC 27101

USA

Phone: +1 336 744 0724

Email: us.sales@hyperstone.com

Hyperstone Asia Pacific - Taiwan

3F., No. 501, Sec.2, Tiding Blvd.

Neihu District, Taipei City 114

Taiwan, R.O.C.

Phone: +886 2 8751 0203

Email: ap.sales@hyperstone.com

www.hyperstone.com

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